

9<sup>th</sup> IEEE Workshop on  
Design and Diagnostics  
of Electronic Circuits and Systems

Masarykova kolej  
Prague, Czech Republic  
April 18-21, 2006



#### General Co-Chairs

Bernd Straube  
Fraunhofer IIS/EAS Dresden (DE)  
bernd.straube@eas.iis.fraunhofer.de

Ondřej Novák  
Czech Technical University in Prague (CZ)  
novako3@fel.cvut.cz

#### Programme Chair

Matteo Sonza Reorda  
Politecnico di Torino (IT)  
matteo.sonzareorda@polito.it

#### Programme Vice-Chair

Zdeněk Kotásek  
Brno University of Technology (CZ)  
kotasek@fit.vutbr.cz

#### Organizing Committee Chair

Hana Kubátová  
Czech Technical University in Prague (CZ)  
kubatova@fel.cvut.cz

#### Publicity Chair

Raimund Ubar  
Tallinn Technical University (EE)  
rauib@pld.ttu.ee

#### Steering Committee

E. Gramatová (SK); A. Hławiczka (PL);  
E. Hryniewicz (PL); Z. Kotásek (CZ);  
A. Krasniewski (PL); H. Manhaeve (BE);  
E.J. Marinissen (NL); O. Novák (CZ);  
A. Pawlak (PL); A. Pataricza (chair, HU);  
S. Piestrak (PL); M. Renovell (FR); B. Straube (DE);  
J. Sziray (HU); R. Ubar (EE); K. Vlček (CZ)  
Ex-officio: N. Frištacký (SK)

#### Programme Committee

E. Aas (NO); J. Becker (DE); D. Borrione (FR);  
G. Carlsson (SE); S. Chakravarty (USA);  
R. Drechsler (DE); L. Entrena (ES); J. Figueras (ES);  
N. Frištacký (SK); T. Garbolino (PL); P. Girard (FR);  
M. Glesner (DE); S. Goel (NL); E. Gramatová (SK);  
A. Handkiewicz (PL); S. Hellebrand (AU);  
A. Hławiczka (PL); E. Hryniewicz (PL); L. Jóźwiak  
(NL); Z. Kotásek (CZ); A. Krasniewski (PL);  
K. Kuchcinski (SE); C. Landrault (FR); E. Larsson  
(SE); H. Manhaeve (BE); N. Mukherjee (USA); N.  
Nicolici (CA); F. Novak (SLO); O. Novák (CZ); A.  
Pataricza (HU); A. Pawlak (PL); Z. Peng (SE); S.  
Piestrak (FR); W. Pleskacz (PL); A. Pleštil (CZ);  
P. Prinetto (IT); M. Rencz (HU); M. Renovell (FR);  
B. Rouzeyre (FR); G. Russel (UK); J. Segura (ES); L.  
Sekanina (CZ); O. Sentieys (FR); M. Sonza Reorda  
(IT); J. Sosnowski (PL); A. Steininger (AU); V.  
Stopjaková (SK); B. Straube (DE); J.P. Teixeira  
(PT); I. Teixeira (PT); J. Tyszer (PL); R. Ubar (EE);  
K. Vlček (CZ); H.J. Wunderlich (DE); Y. Zorian  
(USA)

#### Organizing Committee

P. Fišer (CZ); Z. Plíva (CZ); P. Kubalík (CZ);  
J. Škvor (CZ)

## Call for Papers

The **IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems** provides a forum for exchanging ideas, discussing research results, and presenting practical applications in the areas of design, test, and diagnosis of microelectronic circuits and systems.

The **DDECS Workshop** series is organised by Central European countries: Czech Republic (1997, 2002), Poland (1998, 2003), Slovakia (2000, 2004) and Hungary (2001, 2005).

DDECS 2006 is organised by the **Department of Computers** of the **Czech Technical University** in Prague and is sponsored by the **IEEE Computer Society** – **Test Technology Technical Council (TTTC)**.

#### Topics of interest include but are not limited to:

- *ASIC/FPGA Design*
- *Bio-inspired Hardware*
- *Design Verification/Validation*
- *Formal Methods in System Design*
- *Hardware/Software Co-Design*
- *IP-based Design*
- *Logic Synthesis*
- *Physical Design*
- *Reconfigurable Computing*
- *System-on-a-Chip (SoC)*
- *Analog, Mixed-Signal, and RF Test*
- *ATE Hardware and Software*
- *Built-in Self-Test (BIST)*
- *Design for Testability and Diagnosis*
- *Defect/Fault Tolerance and Reliability*
- *Embedded Test*
- *Memory and Processor Test*
- *MEMS Testing*

**Paper submissions:** Prospective authors are cordially invited to submit original papers in English of 6 pages maximum. Electronic submission (using the workshop web page) in PostScript or PDF format is required. Please identify the contact author with complete mailing address, phone and fax numbers, and e-mail address. Special student and industrial sessions will be organised. Accepted papers will be included in the Workshop Proceedings.

#### Important dates:

- **New: submission deadline:** **January 22, 2006**
- Notification of acceptance: **March 5, 2006**
- Camera-ready deadline: **March 19, 2006**

**Workshop location:** The workshop will be held in the beautiful city of Prague, capital of the Czech Republic, which offers its visitors a breathtaking historical environment. The workshop site itself will be the Congress Center of the Czech Technical University called „Masarykova kolej“. Masarykova kolej is very close to the city centre of Prague. Address is: Thákurova 1, Prague 6, CZ.

**For further information** please visit the DDECS 2006 web page:  
<http://ddecs06.felk.cvut.cz>

#### DDECS 2006 contact address:

Hana Kubátová  
Department of Computer Science and Engineering  
Czech Technical University in Prague, Karlovo nám. 13  
121 35 Praha 2, Czech Republic  
Phone: +420 224357281  
E-mail: ddecs06@felk.cvut.cz

